

***A Primer on Verilog
Simulation Using Icarus Verilog,
Cver, Dinotrace and GTKWave***

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Requirements

- ◆ A Computer with Fedora Core 5 or 6 or Cygwin installed in MS Windows. Debian also has Icarus Verilog and GTKWave in its repository. Use your favorite distribution.
- ◆ Dinotrace uses Motif widgets. So, check whether you have Motif before installing it.
- ◆ Get accustomed to typical GNU/Linux environment and learn the main shell commands and scripting, as it can help in automating tasks.

Installing the Tools from Source

- ◆ Read the INSTALL and/or README file in the extracted directory to know exactly how to install the tool.
- ◆ Well, installation steps are generally same as what one does while installing any software from source - `./configure ; make ; make install`
- ◆ For Cver, only run, “**\$ make -f file all**” to generate binaries in bin directory. Either copy the binaries to `/usr/bin` or create aliases in a shell init file, like `.bashrc` for bash.

Steps for Verilog Simulation

- ◆ Write the error free Verilog code for your model / logic / circuit / hardware / algorithm / whatever...
- ◆ Write the suitable test bench code for the module with commands for generating the Value Change Dump (VCD) file.
- ◆ Run `cver` or `iverilog` to compile your test bench code and use either `Dinotrace` or `GTKWave` for viewing the VCD file thus generated.

Verilog Code of a 4-bit Comparator

```
enjo@205:~/Verilog_Codes
my_4_bit_ripple_counter.v
my_4_bit_ripple_counter.v
my_4_bit_serial_in_parallel.v
my_4_bit_serial_in_parallel.v
my_4_bit_serial_in_parallel.v
my_4_bit_serial_in_parallel.v
my_4_input_nand_gate.v
my_4_input_nand_gate.v
my_8_to_3_priority_encoder.v
my_8_to_3_priority_encoder.v
my_commercial_d_flip_flop.v
my_commercial_d_flip_flop.v
my_simple_inverter_gate.v
my_simple_inverter_gate.v
test2.vcd
test.vcd
Verilog_Autosim
Verilog_Autosim.c
Verilog_Autosim.o
verilog_autosim_script
verilog.log
Verilog_Test_testbench
Verilog_Test.v
]$
Trying other mirror.
http://gulus.USherbrooke.ca/pub/distro/
ate: Sat, 22 Dec 2007 12:27:05 GMT
Server: Apache/1.3.26 (Unix) Debian GNU
Transfer-Encoding: chunked
Content-Type: text/html; charset=iso-88
Trying other mirror.
primary.xml.gz          100% |=====
updates : ##### 1085/1085
Added 241 new packages, deleted 171 old in 23.54 seconds
0 packages excluded due to repository protections
Parsing package install arguments
Resolving Dependencies
[]

my_4_bit_comparator.v (~/Verilog_Codes) - GVIM
File Edit Tools Syntax Buffers Window Help
`timescale 1ns / 1ps
module my_4_bit_comparator (InA, InB, A_Great_B_OutY, A_Less_B_OutY, A_Equal_B_OutY);
input [3:0] InA, InB;
output reg A_Great_B_OutY, A_Less_B_OutY, A_Equal_B_OutY;
always @(InA or InB)
  if (InA == InB)
    begin
      A_Great_B_OutY = 1'b0;
      A_Less_B_OutY = 1'b0;
      A_Equal_B_OutY = 1'b1;
    end
  else if (InA < InB)
    begin
      A_Great_B_OutY = 1'b0;
      A_Less_B_OutY = 1'b1;
      A_Equal_B_OutY = 1'b0;
    end
  else if (InA > InB)
    begin
      A_Great_B_OutY = 1'b1;
      A_Less_B_OutY = 1'b0;
      A_Equal_B_OutY = 1'b0;
    end
end
endmodule
~
27,9 All
```

Test Bench for the 4-bit Comparator

```
File Edit View Terminal Tabs Help
timescale 1ns / 1ps
include "my_4_bit_comparator.v"
module my_4_bit_comparator_tb;

reg [3:0] InA_T, InB_T;
wire A_Great_B_OutY_T, A_Less_B_OutY_T, A_Equal_B_OutY_T;

my_4_bit_comparator UUT (.InA(InA_T), .InB(InB_T), .A_Great_B_OutY(A_Great_B_OutY_T),
                        .A_Less_B_OutY(A_Less_B_OutY_T), .A_Equal_B_OutY(A_Equal_B_OutY_T));

initial
begin
    $dumpfile("four_bit_comparator.vcd");
    $dumpvars(2, my_4_bit_comparator_tb.UUT);
end

initial
begin
    InA_T = 4'h0; InB_T = 4'h0;
end

always
begin
    forever #5 InA_T[0] = ~InA_T[0];
end
always
begin
    forever #10 InA_T[1] = ~InA_T[1];
end
always
begin
    forever #20 InA_T[2] = ~InA_T[2];
end
always
begin
    forever #40 InA_T[3] = ~InA_T[3];
end
always
begin
    forever #80 InB_T[0] = ~InB_T[0];
end
always
begin
    forever #160 InB_T[1] = ~InB_T[1];
end
always
begin
    forever #320 InB_T[2] = ~InB_T[2];
end
always
begin
    forever #640 InB_T[3] = ~InB_T[3];
end

initial
begin
    #1280 $finish;
end
endmodule
```

Include the module to be tested in the test bench code

Named port mapping

Instantiation of Design Module

Dump the variables of the instantiated module, at the 2nd level of hierarchy

Test vector initialization and generation

Commands for Compilation

cver on compilation of the test bench code will generate the VCD file :

```
]$ cver +verbose -informs my_top_module.v
```

or

For compiling the code using Icarus Verilog, run the command :

```
]$ iverilog -v my_top_module.v
```

which results in generation of an executable file which is executed by :

```
]$ ./a.out
```

to generate the .VCD file.

Viewing the VCD File

View the dumped results on the waveform viewer by running :

```
]$ gtkwave dumpfile_name &
```

or

```
]$ dinotrace dumpfile_name &
```

Waveforms on GTKWave

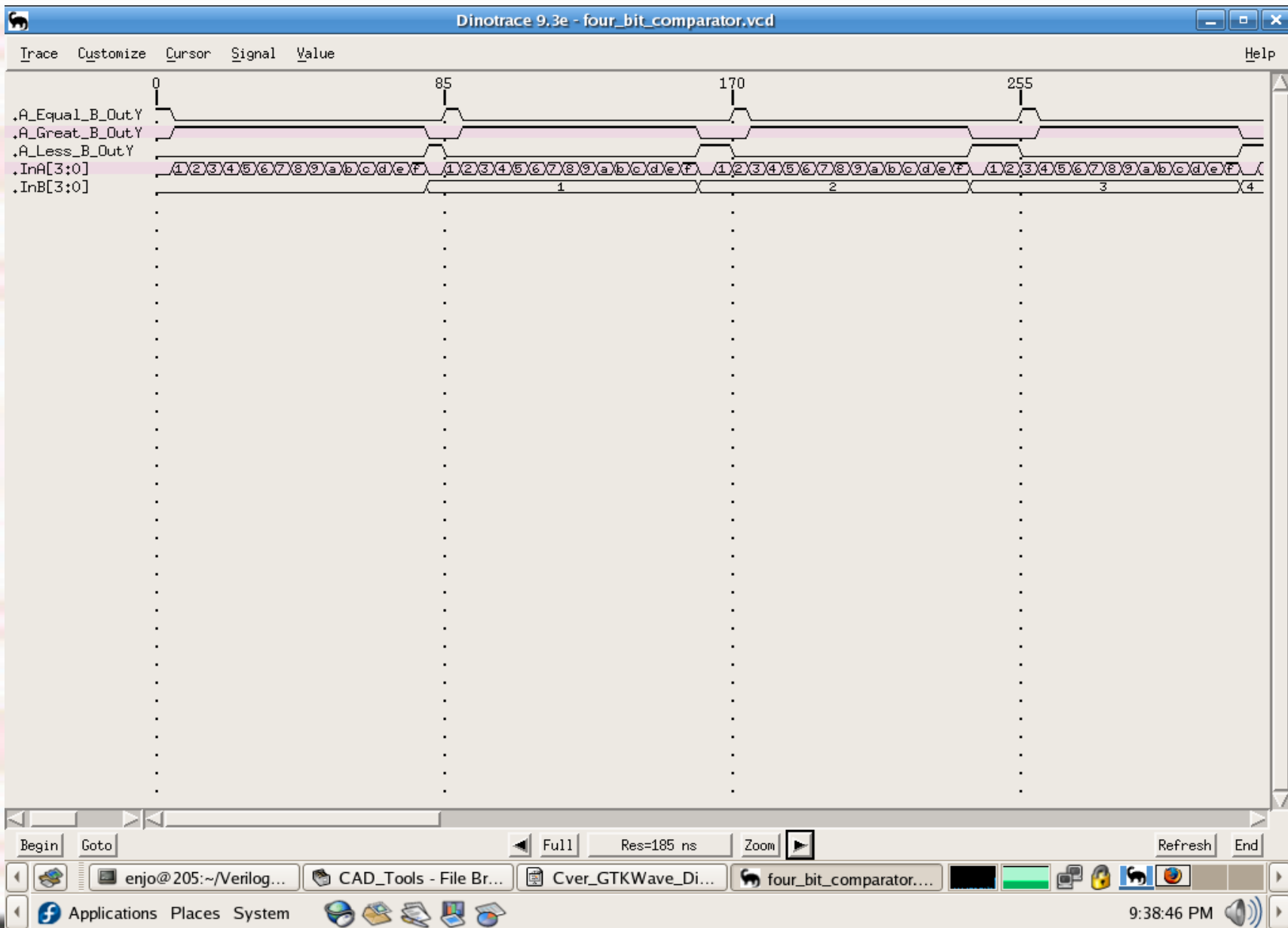
The screenshot displays the GTKWave interface for a Verilog simulation. The window title is "GTKWave - four_bit_comparator.vcd". The menu bar includes File, Edit, Search, Time, Markers, View, and Help. A status message on the left indicates "VCD loaded successfully. [5] facilities found. Regions formed on demand." The toolbar contains various navigation and zooming tools. The "Marker Time" is 151400 ps and the "Current Time" is 0 sec. The "From" time is 0 sec and the "To" time is 1280 ns.

The main workspace is divided into three panels:

- SST (Signal Structure Table):** Shows a tree view with "my_4_bit_comparator_tb" expanded to "L UUT".
- Signals:** Lists the current signals: InA[3:0]=E, InB[3:0]=1, A_Equal_B_OutY=0, A_Great_B_OutY=1, and A_Less_B_OutY=0.
- Waves:** Displays a digital waveform with a 100 ns scale. The top row shows a hexadecimal time scale (0-9, A-F). The signals are plotted as digital waveforms: InA[3:0] is constant at 'E', InB[3:0] is constant at '1', and the three output signals (A_Equal_B_OutY, A_Great_B_OutY, A_Less_B_OutY) show logic-level transitions corresponding to the comparison of 'E' and '1'.

At the bottom, the system tray shows the user "enjo@205:~/Verilog...", open files, and the system clock at 9:45:13 PM.

Waveforms on Dinotrace



References

- ◆ Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”
- ◆ Jayaram Bhasker, “Verilog HDL Synthesis, A Practical Primer”
- ◆ Michael Ciletti, “Advanced Digital Design With Verilog HDL”
- ◆ Documentation provided with Cver in doc directory
- ◆ Documentation provided with GTKWave in doc directory
- ◆ http://iverilog.wikia.com/wiki/Main_Page
- ◆ <http://www.veripool.com/dinotrace/doc.html>