

Verilog®HDL Simulation Assignment - I

- 1.) Write a behavioral Verilog HDL code for a D-Flip Flop with synchronous preset and asynchronous clear. Test it using a test bench.
- 2.) Write separate behavioral Verilog HDL codes for all the basic gates. Write the structural code for a 1-bit full adder by instantiating the written modules of the required gates in the design. Also write a behavioral code for the adder without using any gates. Test them using a test bench.
- 3.) Write a behavioral Verilog HDL code for a 4-bit Parallel In Serial Out shift register, which will accept the next 4-bits of data only after serially shifting the previously inputted 4 bits. Of course, test it using a test bench.

NB -

- 1.) All students will E-Mail me their assignment solutions before the deadline, which is December 30th of 2007 23:59:59 hours, Indian Standard Time. Actually, the too much of time is given for finishing these assignment questions. So, I expect all the solutions way ahead of the deadline.
- 2.) Deliverables include HDL codes, test benches and .VCD files.
- 3.) Test benches for all the codes is a must and make sure that your stimuli verifies all the input combinations. That is, I need 100% coverage for the above questions.
- 4.) All the students will send me the generated .VCD files along with their Verilog design and test bench codes.
- 5.) All the students will individually explain their codes.
- 6.) Remember that there are marks for this assignment. So, be very serious in doing it and submitting them before the deadline.