

January 26th of 2008

Verilog®HDL Simulation Assignment - II

- 1.) Write a behavioral Verilog HDL code for a parametrized up/down counter with a load input and count enable input. Test it using a test bench for 6-bit counter operation.
- 2.) Write a behavioral Verilog HDL code for a parametrized ring counter with a count enable input. Test it using a test bench for 6-bit ring counter operation.
- 3.) Write a behavioral Verilog HDL code for a parametrized Johnson counter with a count enable input. Test it using a test bench for 6-bit Johnson counter operation.

NB -

- 1.) All students will E-Mail me their assignment solutions before the deadline, which is February 2nd of 2008 23:59:59 hours, Indian Standard Time. I expect the solutions from all the students, way ahead of the deadline.
- 2.) Deliverables include HDL codes, test bench codes and .VCD files.
- 3.) Test benches for all the modules is a must and make sure that your stimuli verifies all the state combinations possible. That is, I need 100% state coverage for the above questions.
- 4.) Please remember to put the question as a comment in the beginning of every code.
- 5.) Please do not send me the individual files attached with the E-Mail as the readable files can get added to the body of the message and it will waste a lot of time for one to scroll down for getting every file. So, attach the compressed archive (preferably as .tar.gz or .tar.bz2 or .tgz or .gz or .bz2) of all the files with the E-Mail and not all the files individually.
- 6.) All the students will have to individually explain their codes.
- 7.) Remember that there are marks for this assignment. So, be very serious in doing it and submitting them before the deadline.
- 8.) All the Debian GNU/Linux machines of college Computer Centre have been installed with Icarus Verilog, GHDL and GTKWave, thanks to Mr. Titty Jacob. So, you need not depend only on the project Laptops with tools installed or on the Digital Communication Laboratory machines to do your assignment.