

**Verilog®HDL RTL Coding Assignment - III**

- 1.) Write an RTL code for a parametrized combinational N-bit barrel shifter. Test it using an appropriate test bench for 32-bit barrel shifting. ζ
- 2.) Write an RTL code for implementing a parametrized N:1 multiplexer with enable input. Test it using an appropriate test bench for 64:1 multiplexing. ζ
- 3.) Write an RTL code for a parametrized N-bit Gray code counter. Test it using an appropriate test bench for its .
- 4.) Write an RTL description for a parametrized combinational N-bit unsigned comparator with “greater than”, “less than” and “equal to” outputs. Verify the functionality of the code for its 10-bit operation. ζ
- 5.) Write an RTL code for implementing a parametrized N-bit adder/subtractor module with carry in/borrow in input. Test the logic for 8-bit operation. ζ
- 6.) Write an RTL code for implementing a signed adder that adds a 16-bit signed number to an 8-bit signed quantity, producing a 17-bit result. Write an appropriate test bench to functionally verify the logic. ζ
- 7.) Write an RTL description for implementing a parametrized N-bit binary decoder and test its functionality for 8 to 256 decoding operation. ζ
- 8.) Implement a parametrized N-bit parity generator providing an odd and even parity output. Functionally verify the logic using a test bench for 8-bit parity generation.
- 9.) Write an RTL description for an 8-bit priority encoder which has its priority decreasing from the least significant bit of the active-HIGH input to the most significant bit of the input.
- 10.) Write a Verilog description for implementing a stop watch with START, STOP and RESET buttons. Test the functionality using a test bench for arbitrary input patterns.

NB -

- 1.) Deliverables include HDL codes, test bench codes and .VCD files. Test benches for all the modules is a must and make sure that your stimuli verifies all the state combinations possible.
- 2.) Please remember to put the question as a comment in the beginning of every code.
- 3.) All the students will have to individually explain their codes.
- 4.) All the Debian GNU/Linux machines of college Computer Centre have been installed with GPL Cver, GHDL and GTKWave, thanks to Mr. Titty Jacob. So, you need not depend only on the project laptops with tools installed or on the Advanced Projects Laboratory machines to do your assignment.