

December 26th of 2008**Verilog@HDL RTL Coding Assignment - IV**

- 1.) Write an RTL code for a parametrized universal counter/shift register. The counter should also generate a terminal count output. Test it using an appropriate testbench for 8-bit operation.
- 2.) Write an RTL code for implementing a parametrized M by N memory with a Read/ $\overline{\text{Write}}$ input. The module should have bidirectional I/O pins to write and read. Verify the functionality for a 1024 byte memory using an appropriate testbench.
- 3.) Draw the state diagram for a Moore machine and also for a Mealy machine that sequentially decodes the pattern "abba" from an input stream that would consist of a's and b's only. Write an RTL for the Mealy and Moore machines. Verify the sequential decoding using a testbench.
- 4.) Implement the state following diagram, Fig. IV-1 for a Mealy machine using Verilog. The RTL has to implement a registered Mealy machine. Verify the description using a suitable testbench.

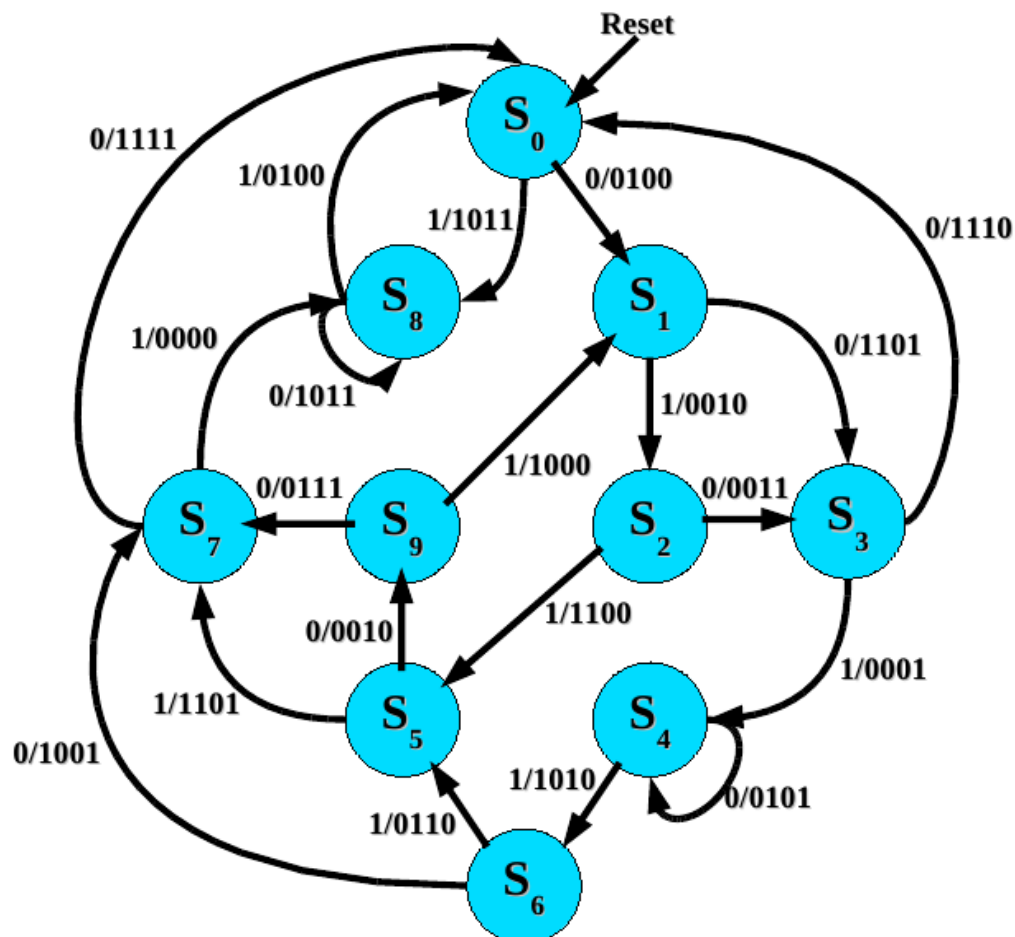


Fig. IV-1 Implement the RTL for the Registered Mealy Machine

- 5.) A vending machine needs to be designed for selling the platform tickets in railway stations. Each platform ticket costs Rs. 3/-. Users are allowed to enter one rupee, two rupee or five rupee coins. But the sum of any coin entry cannot be more than Rs. 6. Coin entries resulting in a sum of Rs. 3 or Rs. 6 are valid and would immediately result in the printing one or two platform tickets respectively. If the input of coins exceeds Rs. 3 or Rs. 6, then the balance has to be returned to the user. Anytime before attaining a sum of Rs. 3 or Rs. 6, user can RESET the machine and get back inputted coins. But once the valid sums have been inputted, ticket(s) may be printed and the balance money if any would be returned to the user. Draw a Moore and Mealy state machine for the vending machine and write efficient RTL descriptions for both for their implementation on an FPGA. Verify the functionality of the description using a suitable testbench. Registered Moore and Mealy implementations are expected.

NB -

- 1.) Deliverables include RTL codes, test bench codes and .VCD files. Test benches for all the modules is a must and make sure that your stimuli verifies all the state combinations possible.
- 2.) Every code has to be synthesizable and Verilog RTL coding guidelines have to be strictly followed.
- 3.) Every code segments has to be properly commented.
- 4.) Please remember to put the question as a comment in the beginning of every code.
- 5.) All the students will have to individually explain their codes.
- 6.) All the Debian GNU/Linux machines of college Computer Centre have been installed with GPL Cver, GHDL and GTKWave. So, you need not depend only on the project laptops with tools installed or on the Advanced Projects Laboratory machines to do your assignments.