

Workshop

on

**“Verilog® HDL and FPGA
Prototyping”**

22nd June – 27th June, 2009

Organized by



**Celebrating 125 years
of Engineering the Future**

IEEE Student Branch

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About MEC

Model Engineering College, Thrikkakara is a premier institute of engineering that has carved a niche for itself in the field of technical education in a very short span of time. Since its inception in 1989, under the aegis of the Institute of Human Resource Development, IHRD (Government of Kerala undertaking), the college has made its presence felt in the technical horizon of the state.

The college offers engineering courses in Computer Science & Engineering, Electronics & Communication Engineering and Electronics & Biomedical Engineering. All eligible programs offered by the college are accredited by National Board of Accreditation (NBA). The college is also funded by Technical Education Quality Improvement Programme (TEQIP) of Government of India.

Objective

Hardware description languages (HDLs) have deeply influenced the VLSI design flow of integrated circuits. Verilog® HDL is a widely used HDL for FPGA and ASIC designs. Field Programmable Gate Arrays (FPGAs) enable rapid prototyping and implementation of

reconfigurable digital hardware. Advanced FPGA devices can accommodate million gate logic designs for signal processing, high speed communication systems and embedded systems applications. The course aims to impart Verilog coding skills for FPGA based system design.

Workshop Contents

- Verilog® HDL simulation and synthesis
- Free open source EDA tools – GPLCver, Icarus Verilog and GTKWave
- Verilog RTL Coding Guidelines
- Hands-on sessions on rapid prototyping using Xilinx FPGA devices

Resource Person

Mr. Cejo K. L., Chairperson, IEEE Kerala Section GOLD Affinity Group, is an IEEE National Distinguished Lecture Program (NDLP) speaker.

Eligibility

Students and faculty members from technical institutions are eligible for the workshop.

How to Apply

The **number of seats are limited to 35** and will be **filled on a first-come first-served basis**. Fill the application form available at the URL given below and E-Mail it to the contact persons mentioned below before 20th June of 2009. Selected participants will be intimated by E-Mail and will have to pay the workshop fees by cash on the opening day of the workshop. The course fee is Rs. 800/- and IEEE members can avail 50% discount on course fee by registering with their IEEE membership number. IEEE members claiming discount will have to produce their IEEE badge on days of workshop. The course fee includes lunch and refreshments during the workshop days. Accommodation will not be provided. Application form and details can be found at the following website:

http://www.mec.ac.in/home/ec/cejo/web/IEEE_TWMM_2009/FP.htm

NB: Last Date for receipt of filled application forms is 20th June of 2009.